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ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
CHEN, JUNPENG	
ART UNIT	**PAPER NUMBER**
2618	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/509,753	Applicant(s) YAMAWAKI ET AL.	
	Examiner Junpeng Chen	Art Unit 2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to applicant's arguments/amendment filed on 12/18/2006. **This action is made FINAL.**

Response to Arguments

2. Applicant's arguments filed 12/18/2006 have been fully considered but they are not persuasive.

In response to applicant's first argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a 2nd-order filter) are not recited in the rejected claim(s) prior to the First Non-Final Rejection. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In response to applicant's second argument that "Midtgaard does not include the detailed description of a loop filter. Therefore, the optimization of the structure is not performed and it can be expected that the noise to be generated is larger than that in Applicant's invention". However, Midegaard in view of Tachimori discloses the loops filters as claimed, the teaching by Midegaard in view of Tachimori is expected to perform as Applicant's claimed invention.

All claimed limitations prior to the First Non-Final Rejection are taught by cited references. Therefore, all prior art rejections in the First Non-Final Rejection are proper and, consequently, are maintained.

Response to Amendment

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 6-7 and 9 are rejected under 35. U.S.C. 103(a) as being unpatentable over **Midtgaard et al. (U.S. PGPub 2002/0090921 A1)** in view of

Tachimori (U.S. PGPub 2002/0051508 A1), and in further view of **Buchwald**, "**A 6-GHz integrated phase-locked loop using AlGaAs/GaAs heterojunction bipolar transistors**", Volume: 27 Issue: Dec. 12 1992, pages: 1752-1762.

Consider **claim 1**, Midegaard et al. discloses a transmitter comprising:

a phase control loop (read as the phase path which comprises voltage controlled oscillator 41, power amplifier 33, mixer 44, low pass filter 45, limiters 37 and 38, phase detector 39 and Loop filter 40, paragraph [0048], Fig. 5), for controlling a phase of a carrier being output from a transmission oscillator (read as voltage controlled oscillator 41, (paragraphs [0046] to [0048]), Fig. 5); and

an amplitude control loop (read as the amplitude path which comprises power amplifier 33, mixer 44, low pass filter 45, envelope detectors 27 and 28, comparator 29, loop filter 30 and envelope controller 31, paragraph [0048], Fig. 5) for controlling an amplitude of a transmission being output signal output from a power amplifier (read as the power amplifier 33, (paragraphs [0046] to [0048]), Fig. 5)

However, although Midegaard et al. discloses a current-output circuit (the circuit combination of envelope detectors 27 and 28 and comparator 29, Fig. 5) in the front stage of the filter (loop filter 30, Fig. 5) and discloses that this filter could be Type II filter with two poles (paragraph [0049]), Midegaard et al. failed to specifically disclose that wherein the filter provided on the amplitude control loop (the examiner interprets this filter as a loop filter inside a control loop) for restricting a frequency band of said amplitude control loop is configured by a first <u>2nd – order</u> passive filter including a capacitor and a resistor and a second passive filter including only a capacitor, and

current-output circuit are provided at the respective front stages of said first passive filter and said second passive filter.

In related art, Tachimori discloses a loop filter in a control loop, which comprises filter 3 and filter 4 (paragraph [0164], Fig. 1). The examiner notices that filter 4 includes a resistor RLP and capacitor CLP. However, it is well known in the art that even without the resistor RLP (current-output type circuit), capacitor CLP itself that is being connected to the ground line would still perform as a low pass filter. Thus, the examiner interprets that resistor RF1 in series connection with capacitor CF1 is a first passive filter with lag-lead characteristic and capacitor CLP itself being connected to the ground line is a second passive filter, which including ONLY one capacitor. Also, resistor RLP is interpreted as a current-output circuits at the front stage of the second passive filter.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teachings of Tachimori on loop filter into the teachings of Midegaard et al. for the purpose of being able to easily adjust the parameter values to meet the desired performance of the transmitter.

However, Midegaard, as modified by Tachimori as above, fails to disclose the first passive filter with lag-lead characteristic is a 2^{nd}-order filter.

Nonetheless, in related art, Buchwald discloses the use of a second order filter with lag-lead characteristic (pages 1755-1757) in a circuit loop. As well known in the art, filters that are referred to as 'First Order', 'Second Order', etc., are referred to the number of components (capacitors and inductors) that affect the 'steepness' or 'shape' of the filter's frequency response. That's being said, it would be within the capabilities of

a person with ordinary skill in the art to incorporate the teachings by Buchwald and modify the teachings by Midegaard, which modified by Tachimori, to use second order passive filter as first passive filter by incorporating an additional capacitor into the filter.

Therefore, it is obvious for a person with ordinary skill in the art at the time the invention was made to incorporate the teachings of Buchwald into the teachings of Midegaard, which modified by Tachimori because second order filter does a better job of attenuating higher frequencies.

Consider **claim 2**, Midegaard et al. discloses a transmitter comprising:

a transmission oscillator (read as voltage controlled oscillator 41, Fig. 5) for generating a carrier (read as the output of voltage controlled oscillator 41);

a power amplifier (read as the power amplifier 33, Fig. 5) for amplifying a generated carrier signal;

a phase control loop (read as the phase path which comprises voltage controlled oscillator 41, power amplifier 33, mixer 44, low pass filter 45, limiters 37 and 38, phase detector 39 and Loop filter 40, paragraph [0048], Fig. 5) which includes a phase detector (read as the circuit of limiters 37 and 38 in connection with phase detector 39) for comparing a reference signal (read as RF Input, Fig. 5) and a feedback signal (read as the signal from low pass filter 45) and for outputting a signal corresponding to a phase difference thereof, and which controls a phase of the carrier being output from a transmission oscillator (paragraphs [0046] to [0048]); and

an amplitude control loop (read as the amplitude path which comprises power amplifier 33, mixer 44, low pass filter 45, envelop detectors 27 and 28, comparator 29, loop filter 30 and envelope controller 31, paragraph [0048], Fig. 5) which includes an amplitude detector (envelop detectors 27 and 28 in connection with comparator 29) for comparing a reference signal (read as RF Input, Fig. 5) and a feedback signal (read as the signal from low pass filter 45) and for outputting a signal corresponding to an amplitude difference thereof, and which controls an amplitude of a transmission being output signal output from a power amplifier (paragraphs [0046] to [0048])

However, although Midegaard et al. discloses a current-output circuit (read as a amplitude detector, which comprises envelope detectors 27, 28 and comparator 29, Fig. 5) in the front stage of the filter (loop filter 30, Fig. 5) and discloses that this filter could be Type II filter with two poles (paragraph [0029]), Midegaard et al. failed to specifically disclose that wherein the filter provided on the amplitude control loop (the examiner interprets this filter as a loop filter inside a control loop) for restricting a frequency band of said amplitude control loop is configured by a first <u>2nd – order</u> passive filter with lag-lead characteristics and a second passive filter of a perfect integrator type, and current-output type circuits are provided at the respective front stages of said first <u>2nd – order</u> passive filter and said second passive filter.

In related art, Tachimori discloses a loop filter in a control loop, which comprises filter 3 and filter 4 (paragraph [0164], Fig. 1). The examiner notices that filter 4 includes a resistor RLP and capacitor CLP. However, it is well known in the art that even without the resistor RLP (current-output type circuit), capacitor CLP itself that is being

connected to the ground line would still perform as a low pass filter. Thus, the examiner interprets that resistor RF1 in series connection with capacitor CF1 is a first passive filter with lag-lead characteristic and capacitor CLP itself being connected to the ground line is a second passive filter, which is a perfect integrator type filter as defined by applicants in the abstract for including ONLY one capacitor. Also, resistor RLP is interpreted as a current-output circuit at the front stage of the second passive filter.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teachings of Tachimori on loop filter into the teachings of Midegaard et al. for the purpose of being able to easily adjust the parameter values to meet the desired performance of the transmitter.

However, Midegaard, as modified by Tachimori as above, fails to disclose the first passive filter with lag-lead characteristic is a 2^{nd}-order filter.

Nonetheless, in related art, Buchwald discloses the use of a second order filter with lag-lead characteristic (pages 1755-1757) in a circuit loop. As well known in the art, filters that are referred to as 'First Order', 'Second Order', etc., are referred to the number of components (capacitors and inductors) that affect the 'steepness' or 'shape' of the filter's frequency response. That's being said, it would be within the capabilities of a person with ordinary skill in the art to incorporate the teachings by Buchwald and modify the teachings by Midegaard, which modified by Tachimori, to use second order passive filter as first passive filter by incorporating an additional capacitor into the filter.

Therefore, it is obvious for a person with ordinary skill in the art at the time the invention was made to incorporate the teachings of Buchwald into the teachings of

Midegaard, which modified by Tachimori because second order filter does a better job of attenuating higher frequencies.

Consider **claim 6, as applied to claim 1 above**, Midegaard et al., as modified by Tachimori and Buchwald, further discloses a transmitter,

wherein a first automatic gain controlled amplifier (read as a compensation element, for example, variable gain amplifier, paragraph [0055] to [0056]) is provided on a feedback path from said power amplifier to said amplitude detector in said amplitude control loop path (read as the path between the output of the amplifier 33 and the input to the envelope detector 27, paragraph [0055]); a second automatic gain controlled amplifier (read as a compensation element, for example, variable gain amplifier, paragraph [0055] to [0056]) is provided on a forward path from *said amplitude detector* to said power amplifier in said amplitude control loop (read as the path between comparator 29 and the amplifier envelope control mechanism 31, paragraph [0055] to [0056]); The examiner interprets that circuit connection of envelope detector 27, 28 and comparator 29 as a amplitude detector.

However, Midegaard et al. failed to specifically discloses gains of said first and second automatic gain controlled amplifiers are controlled such that a product of the gain of said first automatic gain controlled amplifier and said gain of the second automatic gain controlled amplifier are kept approximately constant.

Nonetheless, applicants are reminded that in order for the automatic gain amplifiers to work, these amplifiers have to have at least one **variable** in each of them. Thus, the automatic gain amplifiers recited by applicants can also be called as variable

gain amplifiers, which are taught by Midegaard et al. In addition, since these variable gain amplifiers are with variables, it would be easy for a persona with ordinary skill in the art by the time of the invention to vary the variables of these amplifiers to make the product of the gains of these amplifiers to keep approximately constant.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the variable gain amplifiers taught by Midegaard et al. to obtain the same result as applicants' claimed invention because the variable within each amplifier is *variable*.

Consider **claim 7, as applied to claim 1 above**, Midegaard et al., as modified by Tachimori and Buchwald, further discloses a transmitter,

wherein a bias (read as the output from slow modulator 52, paragraph [0052], Fig. 7) is given such that said power amplifier is operated in nonlinear area (non-linear power amplifier) in both of the said first and second operating modes (read as slow modulator 52 sets an optimum power supply voltage for a given output power level, while the bias control arrangement 47, 48 according to the second aspect handles the envelope variation due to modulation, paragraph [0052], Fig. 7).

Consider **claim 9, as applied to claim 1 above**, Midegaard et al., as modified by Tachimori and Buchwald, further discloses the claimed invention and that the transmitter is for a wireless communication system (Figure1 and 2). However, Midegaard et al. fails to expressly disclose a base band circuit for generating a base band signal on the basis of transmission data, and a modulator for performing a phase

modulation and an amplitude modulation in accordance with base band signal generated in said base band circuit.

Nonetheless, it is inherent that the wireless communication device of Midegaard et al. has a base band circuit to generate a base band signal on the basis of transmission data. Further, Midegaard et al. discloses a transmitter which separates the envelope and phase components of an input modulated RF signal into two separate path 19 (envelope path), 20 (phase path, paragraph [0045]). Therefore, it is inherent that there is a modulator exists in such system or apparatus to perform a phase modulation and an amplitude modulation in accordance with a base band signal generated in said base band circuit.

Therefore, claim 9 is rejected for claiming inherent subject matters in the teachings of Midegaard et al., as modified by Tachimori and Buchwald.

Claims 3-5 are rejected under 35. U.S.C. 103(a) as being unpatentable over **Midtgaard et al. (U.S. PGPub 2002/0090921 A1)** in view of **Tachimori (U.S. PGPub 2002/0051508 A1) as applied to claim 1 above**, and in further view of **Buchwald, "A 6-GHz integrated phase-locked loop using AlGaAs/GaAs heterojunction bipolar transistors"**, Volume: 27 Issue: Dec. 12 1992, pages: 1752-1762, and in further view of **Tsutsui et al. (U.S. PGPub 20050218989)**.

Consider **claim 3, as applied to claim 1 above**, Midtgaard et al. in view of Tachimori and Buchwald, discloses the claimed invention but does not disclose expressly a transmitter, wherein in a first operating mode a phase and amplitude modulation by said phase control loop and said amplitude control loop is performed to

transmit a signal; in a second operating mode, a phase modulation by said phase control loop is performed to transmit a signal; and in said first operating mode and said second operating mode said phase control loop is in common used to perform a phase modulation.

In related art, Tsutsui et al. discloses a transmitter (read as the transmitter in a wireless communication system, abstract), wherein a first operating mode a phase and amplitude modulation by said phase control loop and said amplitude control loop is performed to transmit a signal (read as in EDGE mode transmission, the high frequency implements the 8-PSK modulation for rendering phase shift and amplitude shift, paragraph [0037]); in a second operating mode, a phase modulation by said phase control loop is performed to transmit a signal (read as in GSM mode transmission 8-PSK, the high frequency implements the GMSK modulation for rendering phase modulation, paragraph [0037]); and in said first operating mode (read as EDGE mode transmission, abstract) and said second operating mode (read as GMSK mode transmission) said phase control loop (read as the phase control loop exists in the transmitter of the transmission system) is in common used to perform a phase modulation.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teachings of Tsutsui et al. into the teachings of Midtgaard et al. in view of Tachimori and Buchwald, to allow the transmitter in a wireless transmission system to perform dual mode modulation.

Consider **claim 4, as applied to claim 3 above**, Midtgaard et al., as modified by Tachimori, Buchwald and Tsutsui et al., discloses the claimed invention but does not disclose the transmitter, wherein said first passive filter is provided at a front stage thereof prior to said second passive filter.

Nonetheless, Tachimori further discloses first passive filter (read as Lag-Lead filter that includes RF1 and CF1, Fig. 1) is provided at a front stage thereof prior to said second passive filter (read as the low pass filter that include ONLY a capacitor CLP, Fig. 1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to further incorporate the teaching of Tanchimori into the teachings of Midtgaard et al., which modified by Tanchimori, Buchwald and Tsutsiu et al. to provide a second passive filter after the first passive filter for the purpose of reducing the influence of noise.

Consider **claim 5, as applied to claim 4 above**, Midtgaard et al., as modified by Tachimori, Buchwald and Tsutsui et al., discloses the claimed invention with a circuit provided at a rear stage of said second passive filter (read as Envelope controller 31, Fig. 5) but does not expressly disclose the transmitter, wherein said current-output type circuit provided at a front stage of said second passive filter is designed to configure a perfect integrator circuit comprising said current-output type circuit, said second passive filter, and a circuit provided at a rear stage of said second passive filter.

Nonetheless, Tachimori discloses a loop filter that comprises a current-output type circuit (read as resistor RLP, Fig. 1), said second passive filter (read as capacitor CLP, Fig. 1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to further incorporate the teaching of Tanchimori into the teachings of Midtgaard et al., which modified by Tanchimori, Buchwald and Tsutsiu et al. to configure a perfect integrator circuit comprising said current-output type circuit (read as resistor RLP, Fig. 1), said second passive filter (read as capacitor CLP, Fig. 1), and a circuit provided at a rear stage (read as Envelope controller 31, Fig. 5) of said second passive filter for the purpose of increasing the signal-to-noise ratio.

Claim 8 is rejected under 35. U.S.C. 103(a) as being unpatentable over **Midtgaard et al. (U.S. PGPub 2002/0090921 A1)** in view of **Tachimori (U.S. PGPub 2002/0051508 A1) as applied to claim 1 above**, and in further view of **Buchwald**, "**A 6-GHz integrated phase-locked loop using AlGaAs/GaAs heterojunction bipolar transistors**", Volume: 27 Issue: Dec. 12 1992, pages: 1752-1762, and in further view of **Horii et al. (U.S. Patent 5,715,527)**.

Consider **claim 8**, **as applied to claim 1 above**, Midtgaard et al., as modified by Tachimori and Buchwald, discloses the claimed invention but fails to discloses a transmitter, wherein said power amplifier is configured by a field effect transistor, and a voltage generated in said amplitude control loop is applied to one of a drain and a source of said field effect transistor to control a gain of said transistor.

In related art, Horii et al. discloses a power amplifier (read as power amplifier 11, column 5 lines 50-54, Fig. 1) comprises an FET (Field-Effect Transistor), and a generated voltage in an amplitude control loop is applied to one of a drain and a source of said field effect transistor to control a gain of said transistor (read as gain control signal 181 applied to the drain of the FET to increase the gain of the FET, column 5, lines 50-55, Fig. 1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teaching of Horii et al. into the teachings of Midtgaard et al., which modified by Tachimori and Buchwald for the advantage that FET type power amplifier can be easily integrated.

Claim 10 is rejected under 35. U.S.C. 103(a) as being unpatentable over **Midtgaard et al. (U.S. PGPub 2002/0090921 A1)** in view of **Tachimori (U.S. PGPub 2002/0051508 A1) as applied to claim 9 above,** and in further view of **Buchwald**, "**A 6-GHz integrated phase-locked loop using AlGaAs/GaAs heterojunction bipolar transistors**", Volume: 27 Issue: Dec. 12 1992, pages: 1752-1762, and in further view of **Duperray (U.S. PGPub 2003/0095608 A1)**.

Consider **claim 10, as applied to claim 9 above**, Midtgaard et al., as modified by Tachimori and Buchwald, discloses the claimed invention but fails to discloses a wireless communication apparatus wherein a signal for controlling a gain of said first automatic gain control amplifier and a gain of said second automatic gain controlled amplifier is generated in said base band circuit.

In related art, Duperray discloses the signals (read as C1, C2, C3, paragraph [26] Fig. 1) for controlling the gains of variable gain controlled amplifiers (read as variable gain power amplifier 9 and 17, paragraph [26], Fig. 1) are generated in base band circuit (read as base band unit 20, paragraph [26], Fig. 1)

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the teaching of Duperray into the teachings of Midtgaard et al., as modified by Tachimori and Buchwald, to control the gains of automatic gain control amplifiers so the output of the automatic gain control amplifiers will have a desired relationship between them because the gain control signals are from the same source.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a)..

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junpeng Chen whose telephone number is (571) 270-1112. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on 571-272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

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Junpeng Chen
J.C./jc

EDAN ORGAD
PRIMARY PATENT EXAMINER
Edan Orgad 2/5/07